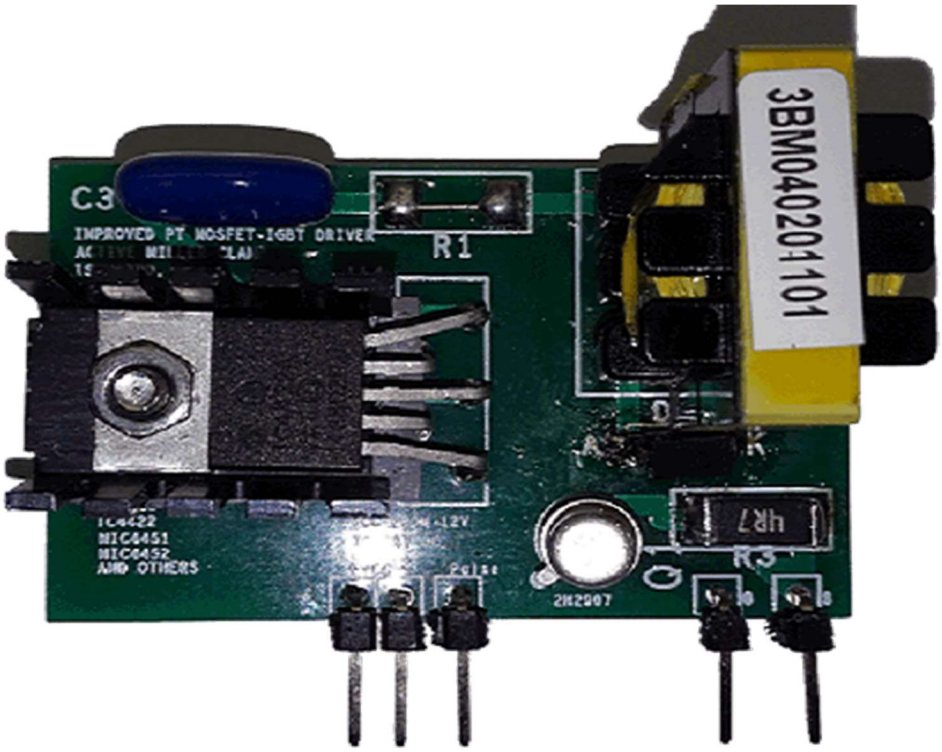
Gate pulse amplifier with pulse transformer Le-T1D12-08



- **Vcc supply voltage between 12 and 18 V**
- **High level input signal: between 2.5 V and Vcc**
- **Low level input signal: less than 1.3 V**
- **Optimum operation between 15 kHz and 200 kHz**
- **Suitable for controlling large Mosfets / IGBTs**
- **Peak current up to 8A**
- **Active Miller Clamp**
- **Compatible with Silicon Carbide Mosfets (SiC Mosfets)**
- **Vertical mounting to reduce space**
- **Supports pulses with PWM modulation. Duty cycle between 0 and 65%**
- **Non-inverting amplifier**
- **1000V insulation voltage.**
- **45mm x 32mm x 25mm**

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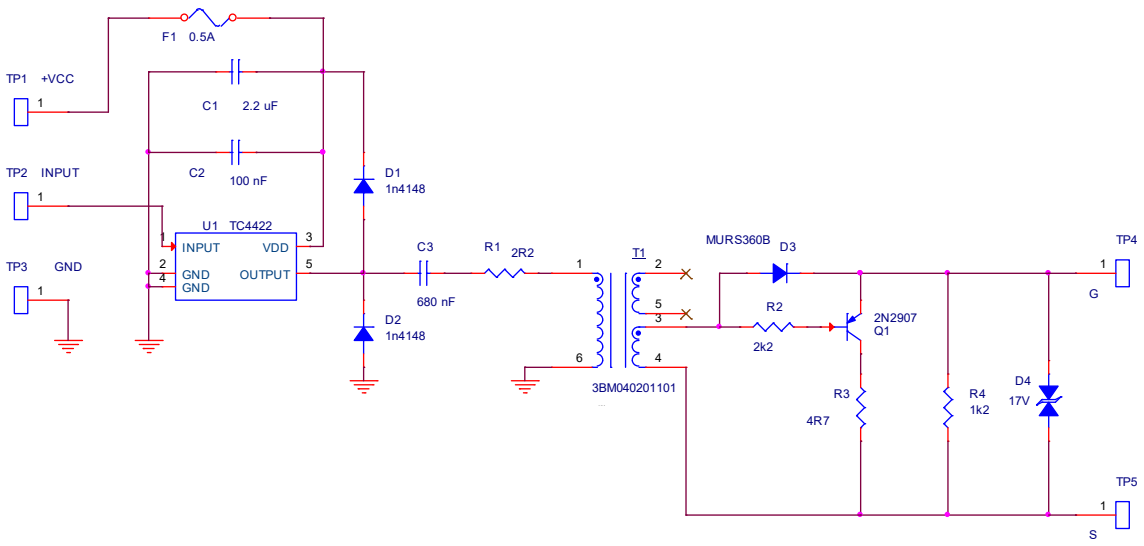

Fig.1. Pulse transformer Gate Driver Schematics.

The T1 transformer has a 1: 2 transformation ratio, to ensure a sufficient amplitude of the driver's output pulses, which makes it possible to work with pulse widths (duty cycle) from zero to 65%. The TVS D4 diode prevents the amplitude of the output pulses from being dangerous for the input circuit of the transistor that is controlled, a situation that could occur for pulse widths below 10%.

The on and off speed of the controlled transistor can be modified with resistors R1 and R3 respectively. With R1 = 0, the minimum ignition time of 30 nanos seconds is obtained.

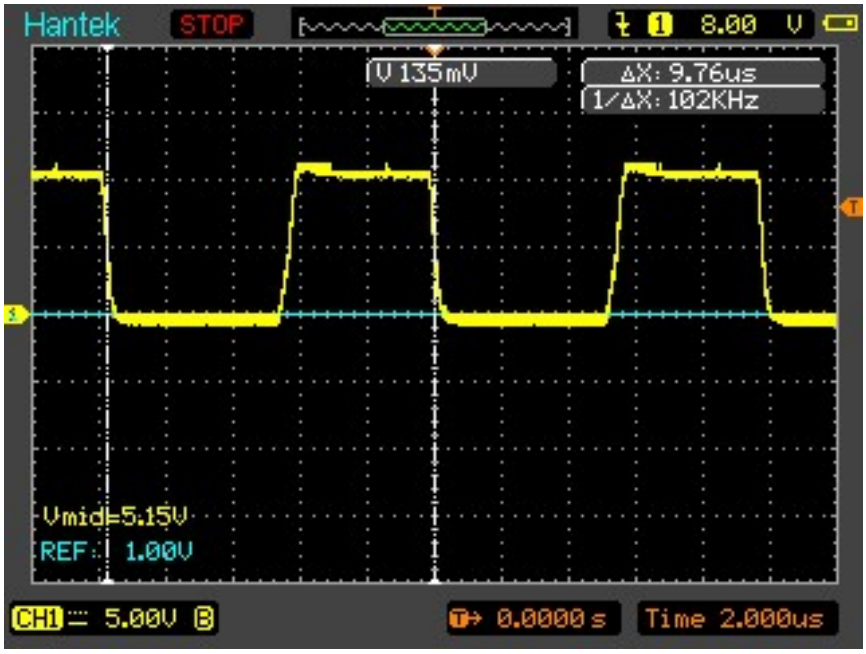

Fig.2. Signal output Vcc 12V and 50 % duty cycle.

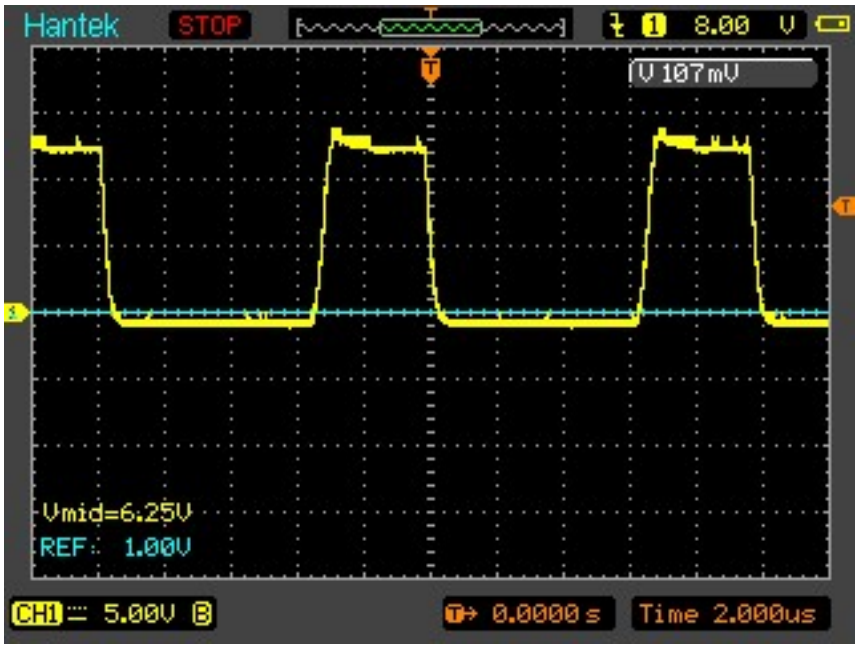

Fig.3. Signal output Vcc 12V and 35 % duty cycle.

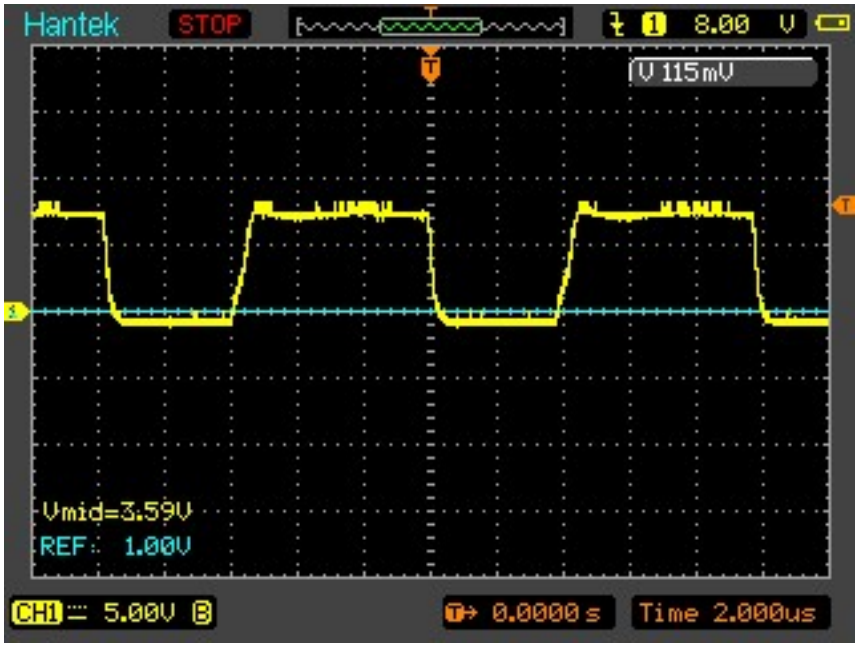

Fig.4. Signal output Vcc 12V and 65 % duty cycle.

The oscillograms show the behavior of the amplifier, controlling a Mosfet of 80 A at a frequency of 102 kHz, for different duty cycle values with Vcc = 12V, R1 = 2R2 and R2 = 4R7.

The operation of the circuit at frequencies above 200 kHz is not recommended, due to a deliberate increase in the power dissipated in the pnp 2n2907 transistor.

In order to operate at frequencies up to 500 kHz, it is necessary to remove transistor Q1, and replace diode D3 with a resistor, but in this case the Miller Clamp function is lost, since there is no one to short-circuit the gate and the source of the transistor controlled during the time it is locked. In this case the circuit would behave like a conventional amplifier with transformer output; the output signal would be symmetric, with positive values in pulse time and negative values in pause time, this is not a problem for the control of conventional Mosfets and IGBTs (as long as the pulse transformer dispersion inductance is low), since the presence of negative voltage at the gate would increase immunity against noise. However, we would also lose compatibility with Silicon Carbide Mosfets (Sic Mosfets). Most of them do not support gate voltages below -5V.

The main disadvantage of the amplifier in fig. 1 is that it lacks the DC level reset. The control circuit has to prevent the pulse width from exceeding 65% of the period, since otherwise the amplitude of the amplifier's output pulses would not be sufficient to guarantee the total opening of the Mosfet or IGBT controlled, and this would die of

excess power.

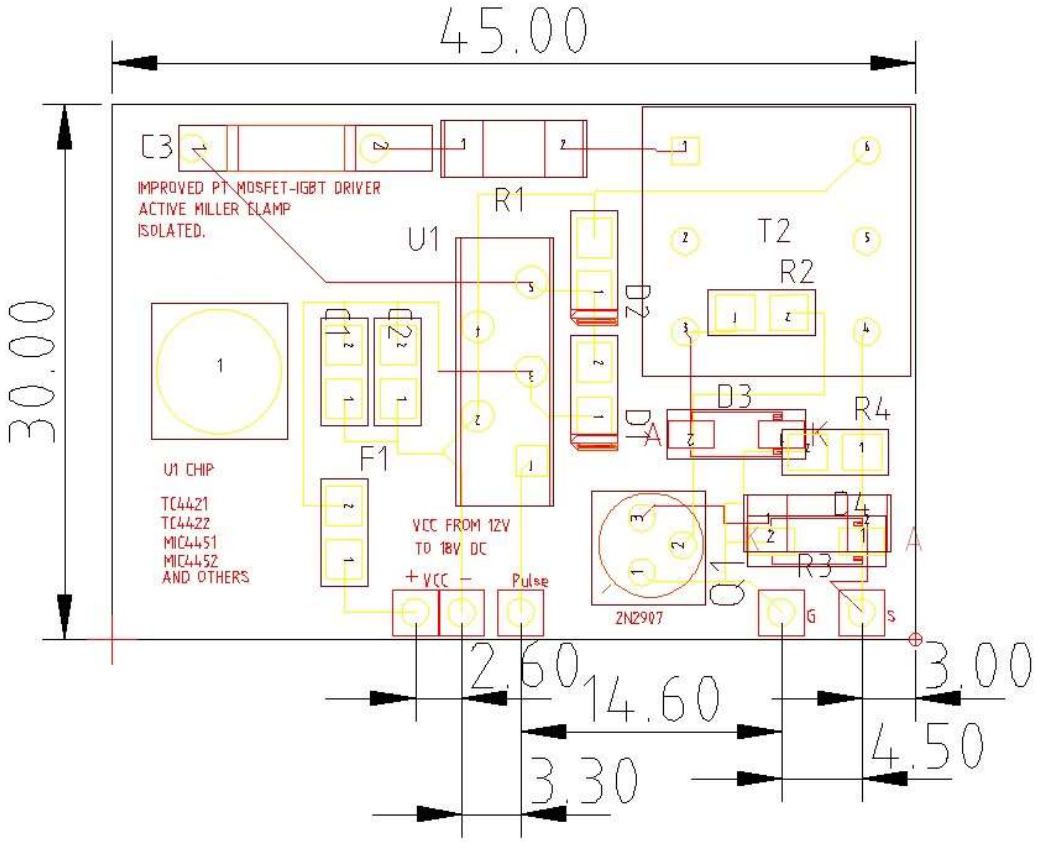

Fig.5. Le-T1D12-08 Outline.