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Power MOSFET
Selecting MOSFFETs and Consideration for Circuit Design

Outline

This document explains selecting MOSFETs and what we have to consider for designing MOSFET circuit, such as temperature characteristics, effects of wire inductance, parasitic oscillations, avalanche ruggedness, and snubber circuit.

Table of Contents

1. Selecting MOSFETs

MOSFETs with appropriate ratings and characteristics should be selected according to the applications in which they will be used.

1.1. Voltage and Current Ratings

The drain-source voltage V_{DSS} rating is important in selecting MOSFETs. Application of a voltage exceeding V_{DSS} might result in the destruction of a MOSFET. It is necessary to choose MOSFETs with a V_{DSS} sufficiently higher than the voltage at which they will actually be used. However, MOSFETs with high V_{DSS} ratings tend to have large on-state resistance, $R_{DS(ON)}$. A downside of using such MOSFETs is increased conduction loss. If you select MOSFETs according to possible peak surge voltage, you could end up opting for devices with large on-state resistance. To address this situation, Toshiba also provides MOSFETs with guaranteed tolerance against avalanche breakdown current or energy in the event that a surge voltage exceeding the voltage rating forces a MOSFET into the breakdown region. Such MOSFETs feature a low V_{DSS} and low on-state resistance.
Generally, on-state resistance determines the upper limit of the drain current I_D. Ensure that not only the loss calculated as $I_D^2 \times R_{DS(ON)}$, the permissible power dissipation but also a temperature rise due to heating does not cause the device to exceed its operating temperature range.

1.2. Considerations for V_{GS}

The conditions governing V_{GS} are also important factors for the selection of MOSFETs. Drain current, $R_{DS(ON)}$ and gate voltage are described below:

(1) The on-state resistance of MOSFETs is low when they operate in the linear region (i.e., at a voltage lower than pinch-off voltage). Therefore, for switching applications, you can reduce the on-state resistance by using MOSFETs in the low V_{DS} region (Figure 1.1). This helps reduce power loss. Note that the amount of current that MOSFETs can handle is limited by the value of V_{GS}.

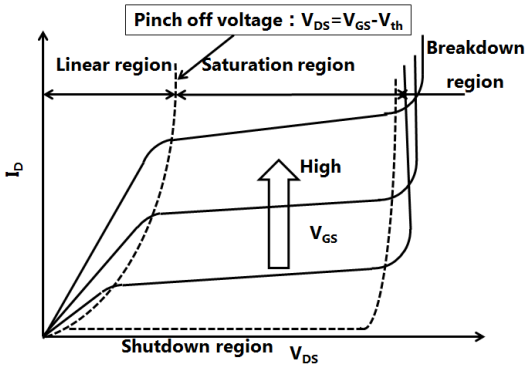


Figure 1.1 Operating Regions of a MOSFET

(2) MOSFETs turn on when the gate-source voltage V_{GS} exceeds their threshold voltage V_{th} (Figure 1.2). It is therefore necessary to choose a value for V_{GS} that is sufficiently higher than V_{th}. There is a tendency that the higher the V_{GS}, the lower the $R_{DS(ON)}$ value becomes. Also, the higher the temperature, the higher the $R_{DS(ON)}$ value becomes (Figure 1.3). In order to reduce loss, it is important to increase V_{GS} in order to minimize the resistance of the device at the current level at which it is used (Figure 1.4). Conversely, a high V_{GS} value increases the drive loss at light loads for high frequency switching. Selecting the optimal gate voltage is therefore critical.

(3) Generally, it is recommended to drive the gate of many power MOSFET at a V_{GS} of 10 V. Toshiba's product portfolio also includes power MOSFETs designed for gate drive at a V_{GS} of 4.5 V. Select the power MOSFET that best suits your equipment requirements.

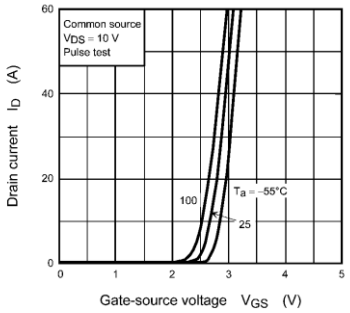


Figure 1.2 I_D-V_{GS} Curves

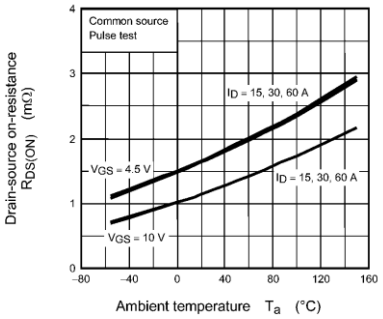


Figure 1.3 $R_{DS(ON)}$-Temperature Curves

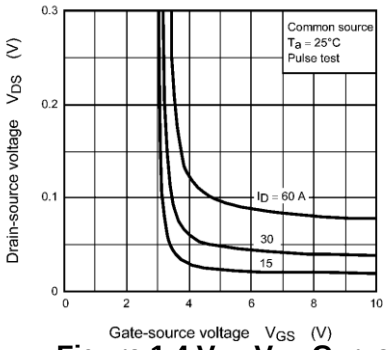


Figure 1.4 V_{DS}-V_{GS} Curves

1.3. **Switching Speed**

When a power MOSFET switches at a high frequency, its switching loss accounts for a significant portion of total loss. To reduce total loss for high frequency switching applications, high speed power MOSFETs should be used.

In our power MOSFETs lineup, in the case of products were classified in low $R_{DS(on)}$ type and high speed type, choose the MOSFETs depend on the application . However if they are not classified, it needs to adjust switching speed by setting output impedance of driving circuit.

2. Considerations for MOSFET Circuit Design

2.1. Temperature Characteristics of Power MOSFETs

The forward transfer admittance $|Y_{fs}|$ of a power MOSFET is given by a differential coefficient of the $I_D - V_{GS}$ curve shown in Figure 2.1.
The temperature coefficient of forward transfer admittance becomes negative in the high current region. Even if large drain current is about to flow due to output change, an increase in internal channel temperature causes forward transfer admittance to decrease, making a power MOSFET less prone to a catastrophic failure due to current concentration and thermal runaway.
What needs to be considered in the use of a power MOSFET is the temperature dependency of drain-source on-state resistance $R_{DS(ON)}$ (Figure 2.2). The temperature coefficient of $R_{DS(ON)}$ varies with the withstand voltage and the manufacturing process of the device. See the appropriate technical datasheet for details. It is therefore necessary to take the temperature dependency of $R_{DS(ON)}$ into consideration in order to select a heat sink with appropriate thermal resistance.

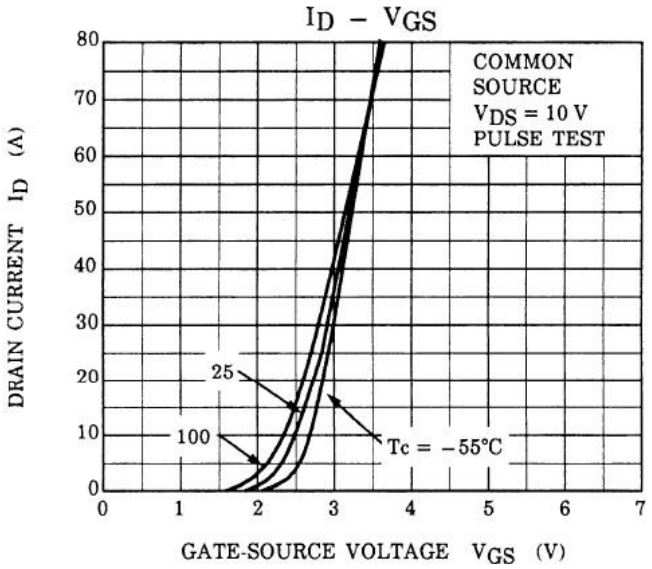


Figure 2.1 I_D – V_{GS} Curves

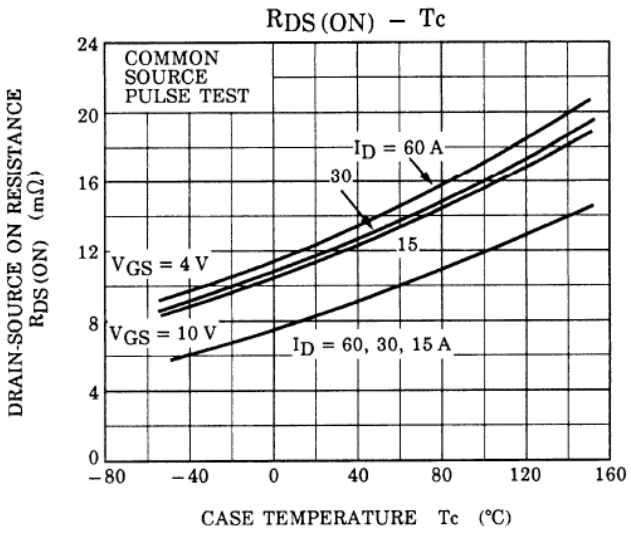


Figure 2.2 $R_{DS(ON)}$ – T_c Curves

2.2. Switching Time and Drive Conditions

Bipolar transistors need a large base current to maintain low on-state voltage. In contrast, since power MOSFETs are voltage-controlled devices, they can be driven just by charging gate capacity, and are therefore a low in power consumption.

Note, however, that power MOSFETs have a slightly large input capacitance C_{iss}. Thus, for high speed switching applications, it is necessary to quickly charge the input capacitance from a low-impedance signal source.

Low-impedance drive is required to reduce turn-on time. However, the use of a high gate voltage results in the much charging of gate-source capacitance, resulting in an increase in $t_{d\ (off)}$.

Switching time can be controlled via gate resistance. If you want to change the turn-on and turn-off switching speeds separately, you can use diodes to change the gate resistance values for turn-on and turn-off. Figure 2.3 shows some examples.

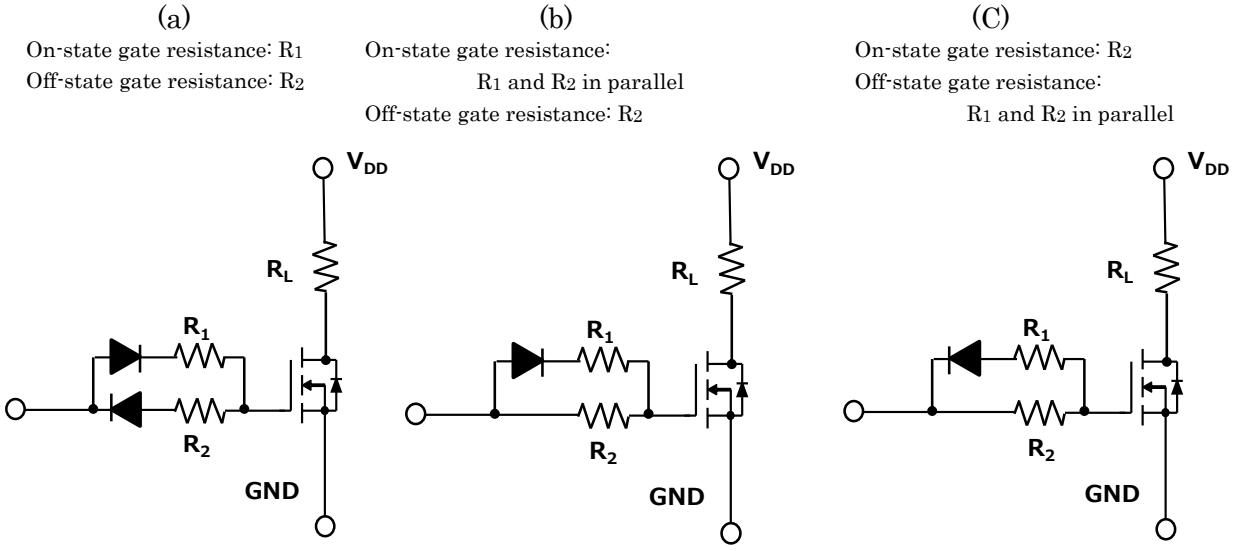


Figure 2.3 Drive Circuit Examples

2.3. Effects of Wire Inductance

Since the switching time of power MOSFETs is more than an order of magnitude lower than that of bipolar transistors, power MOSFETs are ideal for high speed switching applications. However, because of high speed switching performance, a circuit design should be safeguarded against voltage surges so that an excessive surge caused by stray inductances, L_S and L_S', will not be applied to the MOSFET. The surge voltage V_{surge} resulting from stray inductances is calculated as follows:

$$V_{surge} = -(L_S + L_S') \cdot \frac{di}{dt} + V_{DD}$$

It is necessary to ensure that drain-source breakdown voltage V_{DSS} will never be exceeded even in the presence of V_{surge}. V_{surge} can be decreased by reducing di/dt and stray inductances. Since you do not want to reduce di/dt for high speed switching applications, reducing stray inductances are effective. For example, inserting a capacitor as shown in Figure 2.4. is effective to reduce stray inductances.

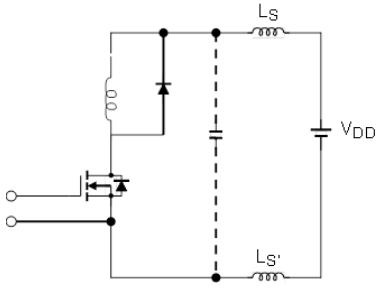


Figure 2.4 Stray Inductances of a Circuit and the Measure

2.4. **Parasitic Oscillations**

Power MOSFETs are more prone to parasitic oscillations than bipolar transistors because of the MOSFET's advantage of high gain in the high frequency domain. A power MOSFET goes into parasitic oscillation when the coupling between input and output increases due to gate-drain capacitance C_{rss} and parasitic wire capacitance C_s causing negative impedance at the input. Several measures are used to prevent parasitic oscillation:

- Use thick, short wires, or use twisted wires to prevent the coupling between two wires.
- Insert a ferrite bead as close to the gate terminal as possible.
- Insert a series resistor in the gate terminal.

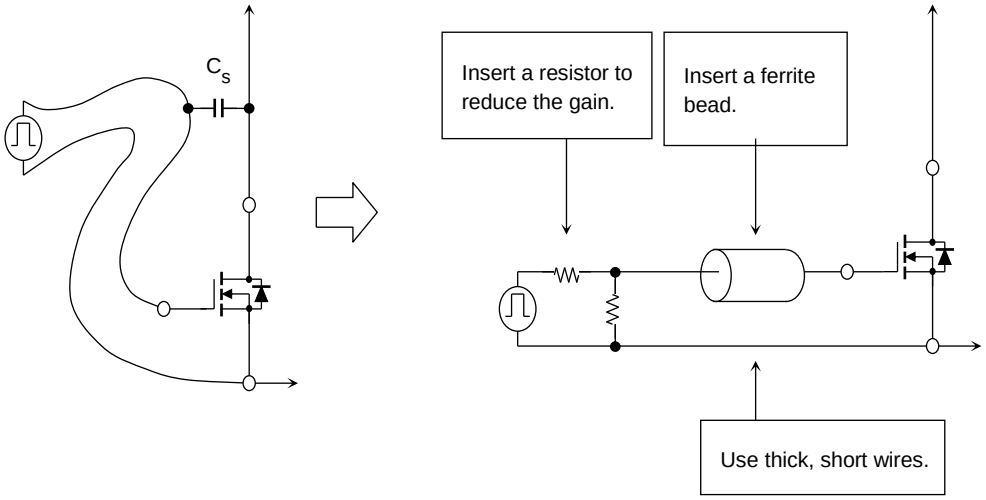


Figure 2.5 Prevention of Parasitic Oscillation

2.5. Use of a Source-Drain Diode

Typical motor control circuits use power MOSFETs in a bridge configuration and alternately turn on and off the MOSFETs upper and lower arms.

When power MOSFETs Q_1 and Q_4 in Figure 2.6 are turned on, a current flows through the circuit, as indicated by A. Next, when MOSFET Q_1 is turned off to control the motor speed, a current circulates through the body diode in MOSFET Q_2 as indicated by B. When MOSFET Q_1 is turned on thereafter, a short-circuit current flows from Q_1 to MOSFET Q_2 as shown by C during the reverse recovery time t_{rr} of the body diode of Q_2. The resulting loss generates heat. Therefore, power MOSFETs having a body diode with a short t_{rr} are desirable for motor control applications. Although body diodes in power MOSFETs can be used as flywheel diodes, MOSFETs with a high speed diode are commonly used for this purpose. In some cases, you can connect a Schottky barrier diode (SBD) in series with a power MOSFET in order to nullify the effect of the body diode in a MOSFET and instead add an external fast-recovery diode (FRD) in parallel with the MOSFET, as shown in Figure 2.7.

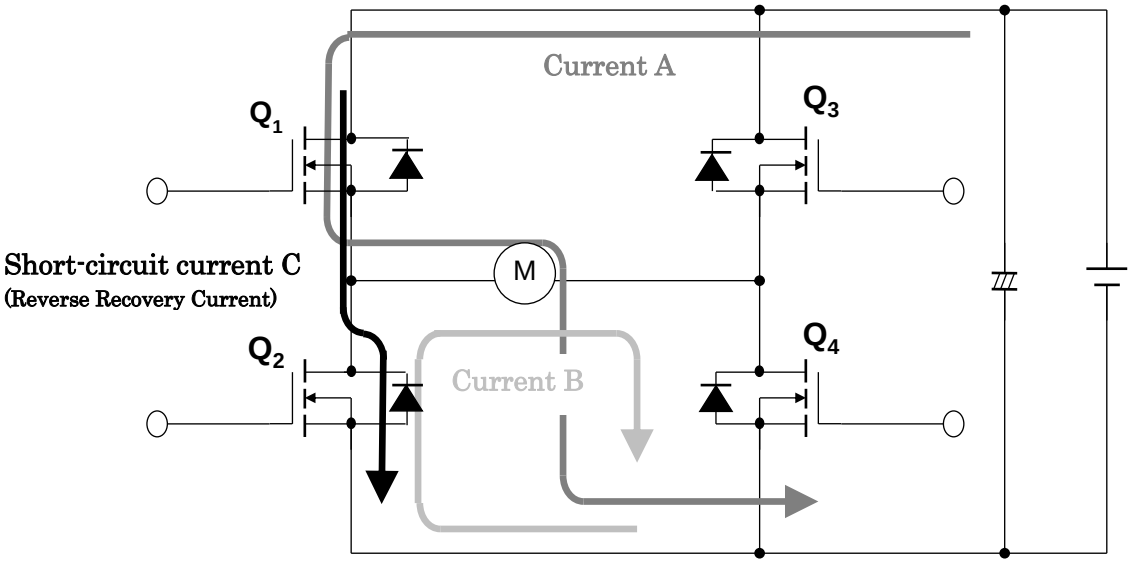


Figure 2.6 Motor Control Circuitry Using Power MOSFETs

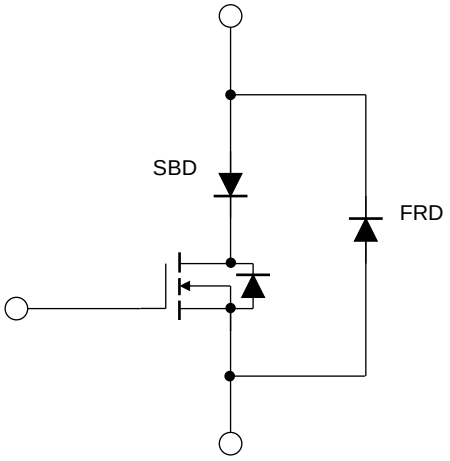


Figure 2.7 Adding External Diodes

2.6. **Avalanche Ruggedness**

Power MOSFETs are commonly used as high speed switching devices. A power MOSFET experiences a high voltage spike between drain and source during device turn-off due to circuit inductance and stray inductances. Sometimes, the spike voltage exceeds the ratings of the MOSFET.
Conventionally, a surge absorber circuit was used to protect electronic devices. Today, surge absorber circuits are dispensed with in order to reduce the number of parts and thereby the size of the system. To address this requirement, a power MOSFET needs to damp avalanche energy even in the event of a voltage surge exceeding its voltage ratings.
In response, Toshiba now provides a product series that can safely operate at up to the self-breakdown voltage as long as avalanche ruggedness conditions are met.
Avalanche events place an excessive stress on the MOSFET. Therefore, even if the avalanche capability is guaranteed, it is recommended to ensure that power MOSFETs will not go into avalanche mode for the sake of system reliability. Note that many MOSFETs do not provide any guarantee for repetitive avalanche ruggedness. For automotive and other safety-critical applications, we urged you to ensure that power MOSFETs, even those with a maximum avalanche energy rating, will not enter avalanche mode. Refer the individual datasheets for details.

- Avalanche energy calculation

Avalanche energy is calculated as:

$$E_{AS} = \frac{1}{2} L {I_{AS}}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

E_{AS}: Avalanche energy
I_{AS}: Avalanche current
BV_{DSS}: Drain-source breakdown voltage
V_{DD}: Supply voltage

Avalanche ruggedness is the energy allowable in a single pulse. The maximum channel temperature, $T_{ch}(max)$, is specified so that the rated avalanche current I_{AS} will not be exceeded when single-shot avalanche energy is applied under the prescribed conditions.
In practice, an increase in temperature caused by an avalanche event is calculated in order to determine that the channel temperature will not exceed the rated $T_{ch}(max)$ value even after ambient temperature, while taking into account a possible rise in temperature caused by steady-state operation and switching losses.
The temperature increase in avalanche mode is estimated as follows:

$$\Delta T_{ch} = 0.473 \cdot BV_{DSS} \cdot I_{AS} \cdot r_{th(ch-c)} \ (Note)$$

BV_{DSS}: Drain-source breakdown voltage
I_{AS}: Avalanche current
$r_{th(ch-c)}$: Transient channel-to-case thermal resistance in avalanche mode

Note: Power dissipation P_D caused by the current and voltage waveforms shown in Figure 2.8 changes over time in the shape of a triangle as highlighted by oblique lines in Figure 2.9. At this time, the channel temperature changes as indicated by the solid line in Figure 2.9, and peaks at time 1/2 t_w. The maximum channel temperature at 1/2 t_w is calculated as 0.699 times the channel temperature change caused by the square wave. Hence, the approximate increase in channel temperature is as follows:

$$\Delta T_{ch} \cong 0.669 \cdot BV_{DSS} \cdot I_{AS} \cdot r_{th}(\frac{1}{2} t_w)$$

$$r_{th}(\frac{1}{2} t_w) \cong \frac{1}{\sqrt{2}} r_{th}(t_w)$$

which can be restated as:

$$\Delta T_{ch} \cong 0.669 \cdot \frac{1}{\sqrt{2}} \cdot BV_{DSS} \cdot I_{AS} \cdot r_{th}(t_w)$$
$$\cong 0.473 \cdot BV_{DSS} \cdot I_{AS} \cdot r_{th}(t_w)$$

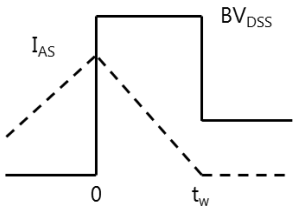


Figure 2.8 Current and Voltage Waveforms

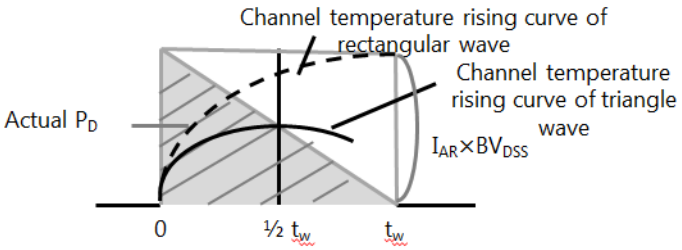


Figure 2.9 Power Dissipation P_D

2.7. **Parallel Connections**

Power MOSFETs have outstanding thermal stability and do not suffer thermal runaway; therefore, connecting them in parallel is easier than with bipolar transistors.
Bipolar transistors are operated by the flow of a base current; therefore, the current balance is disrupted by fluctuations of the base-emitter voltage V_{BE}, making parallel connections difficult. Power MOSFTs, on the other hand, are voltage driven. Therefore it is only necessary to supply drive voltage to each FET connected in parallel, making parallel connection relatively easy. However, when controlling high power at high speeds, it is necessary to carefully consider selection of devices and the range of possible variations in their characteristics. The most important thing to remember when making parallel connections is to avoid current concentration, including overcurrent, and to assure a well-balanced, uniform flow of current to all devices under all possible load conditions.

Normally, current imbalance appears during power-on and power-off; however, this is caused by differences in the switching times of the power MOSFET. It is known that variations in switching times are largely dependent on the value of the gate-source threshold voltage V_{th}. That is, the smaller the value of V_{th} the faster the power-on time. Conversely, during power-off, the larger the value of V_{th}, the faster the cutoff. Because of this, current imbalance occurs during both power-on and power-off when the current concentrates in an FET with a small V_{th}. This current imbalance can apply an excessive power loss of a device and result in failure.
For parallel connections, using of power MOSFETs with close values of V_{th} is preferable in order to reduce variations in switching time during transient periods. It is also important to insert a gate resistor between each power MOSFET connected in parallel to ensure stable operation and prevent abnormal oscillation.(Figure 2.10)

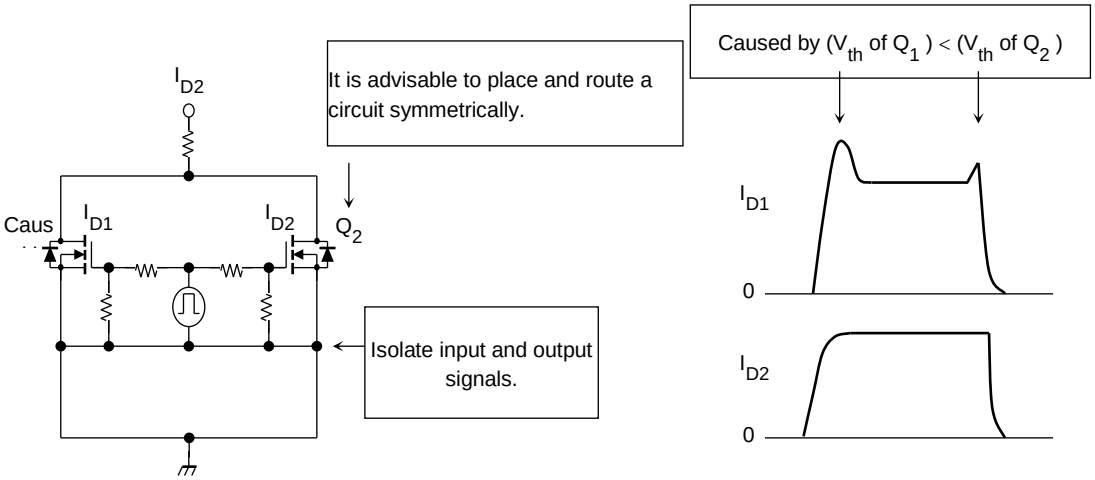


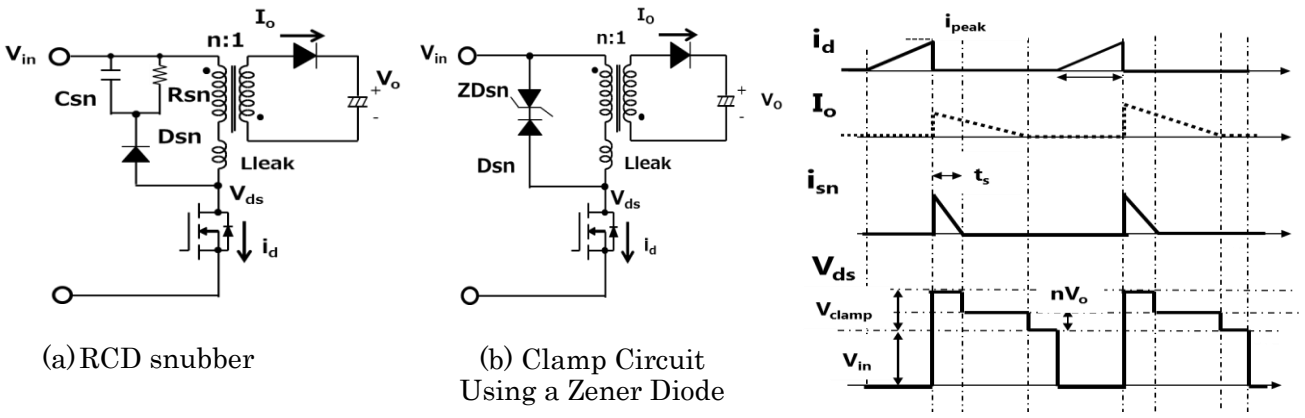
Figure 2.10 Parallel Connection

2.8. Snubber Circuit

Snubber circuits provide protection against transient voltages that occur during turn-off. Generally, a simple RC snubber uses a resistor R in series with a capacitor C. The RC snubber is connected in parallel with a power MOSFET.
Cutting off a current in a circuit causes its voltage to increase sharply due to stray inductances. The snubber damps this surge voltage to protect the power MOSFET as well as components in its vicinity.

2.8.1. Snubber for a flyback converter

Transformers for flyback converters have leakage inductance L_{leak}. Leakage inductance causes a surge voltage to be applied instantaneously across the drain and source terminals of a power MOSFET when the MOSFET turn off. In the worst-case scenario, the surge voltage results in the destruction of the MOSFET.
Snubbers for flyback converters are commonly composed of a diode D and an RC network (Figure 2.11 (a)). The RCD snubber is designed to reduce the effect of parasitic factors that cause a voltage surge. The circuit shown in Figure 2.11 (b) is not a snubber circuit; rather, it is a surge absorber using a clamp circuit.



(a) RCD snubber

(b) Clamp Circuit Using a Zener Diode

Figure 2.11 Leakage Inductance of a Flyback Converter

(1) RCD snubber

An RDC snubber should be designed as follows. Choose a sufficiently large value for C_{sn} so that current ringing during switching can be ignored. Immediately after a MOSFET is turned off, current I_O flows into the secondary coil of the transformer. V_{ds} becomes equal to $V_{in}+nV_o$. (Where, n is the turn ratio, and nV_o is the voltage induced across the primary coil by a current flowing through the secondary coil.) V_{ds} causes a current i_{sn} to flow through the diode D_{sn}. The voltage across L_{leak} becomes equal to $V_{clamp}-nV_o$. At this time, i_{sn} is given by:

$$\frac{di_{sn}}{dt} = -\frac{V_{clamp} - nV_o}{L_{leak}}$$

From this equation, the period of time t_s during which i_{sn} continues flowing is calculated as follows (where, i_{peak} is the peak current that occurs when the MOSFET is turned off.)

$$t_s = \frac{L_{leak}}{V_{clamp} - nV_o} \times i_{peak}$$

The power dissipated by the snubber is:

$$P_{sn} = V_{clamp} \cdot \frac{i_{peak} \cdot t_s}{2} \cdot f_s$$

(where, f_s is the frequency, and $(i_{peak} \cdot t_s)/2] \cdot f_s$ is the current.)

Substituting t_s into this equation gives:

$$P_{sn} = \frac{1}{2} L_{leak} \cdot {i_{peak}}^2 \cdot \frac{V_{clamp}}{V_{clamp} - nV_o} \cdot f_s$$

P_{sn} needs to be consumed by R_{sn} Hence, since

$$\frac{V_{clamp}^2}{R_{sn}} = \frac{1}{2} L_{leak} \cdot {i_{peak}}^2 \cdot \frac{V_{clamp}}{V_{clamp} - nV_o} \cdot f_s$$

R_{sn} is calculated as:

$$R_{sn} = \frac{2V_{clamp}(V_{clamp} - nV_o)}{L_{leak} \cdot {i_{peak}}^2 \cdot f_s}$$

The snubber capacitance C_{sn} should be considered, based on the ripple voltage of the snubber ΔV_{clamp}. Ripple voltage is calculated as follows:

$$\Delta V_{clamp} = \frac{V_{clamp}}{C_{sn} \cdot R_{sn} \cdot f_s}$$

$$\boldsymbol{C_{sn} = \frac{V_{clamp}}{\Delta V_{clamp} \cdot R_{sn} \cdot f_s}}$$

(2) Clamp circuitry using a Zener diode

When a Zener diode is used in a clamp circuit, the Zener clamp voltage, V_z, should be chosen based on a voltage V_{max} sufficiently lower than the maximum switching voltage of the MOSFET and the input voltage V_{in}.

$V_z = Vmax - V_{in}$

The power dissipated by the Zener diode can be calculated in the same manner as for the RCD snubber:

$$P_Z = \frac{1}{2} L_{leak} \cdot {i_{peak}}^2 \cdot \frac{V_{clamp}}{V_{clamp} - nV_o} \cdot f_s$$

This equation shows that if $V_{clamp} - nV_o$ is too low, the power dissipation of the Zener diode increases sharply.

2.8.2. General turn-off snubber

Surge voltage is produced by stray inductances of a circuit. A snubber should be connected in parallel with a switching device to absorb the surge voltage. There are two types of snubbers: one added across each switching device and a lumped snubber added across a power bus for all switching devices.

(1) Snubbers added to each switching device

Cutting off the current in a circuit causes its voltage to increase sharply. Snubbers are designed to reduce a surge voltage to protect a switching device and its surrounding electronic devices.

a. RC snubber circuit

- Ideal for chopper circuits
- The power loss caused by an RC snubber resistor is so large that an RC snubber is not suitable for high frequency switching applications.
- An RC snubber for a high capacitance switching device needs to have a resistor with a small value, which causes drain current to increase during turn-on.
- The power P dissipated by the snubber resistor is calculated as follows:

$$P = C_s \cdot {E_d}^2 \cdot f$$

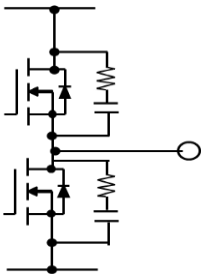


Figure 2.12 RC Snubber

b. RDC charge-discharge snubber

- A diode can be added to the RC snubber to increase snubber resistance. This makes it possible to eliminate a current to be shared by switching devices during turn-on.
- The large power dissipated by the snubber resistor makes an RDC snubber unsuitable for high frequency applications.
- The power dissipated by the snubber resistor is calculated as follows:

$$P = \frac{L \cdot {I_o}^2 \cdot f}{2} + \frac{C_s \cdot {E_d}^2 \cdot f}{2}$$

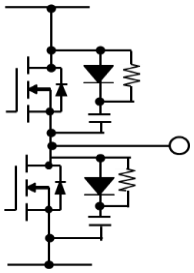


Figure 2.13 RCD Charge-Discharge Snubber

c. Discharge-suppressing RCD snubber

- Turn-off surge voltage is suppressed.
- Ideal for high frequency switching applications.
- The power dissipated by a snubber is small.
- The power P dissipated by the snubber resistor is calculated as follows:

$$P = \frac{L \cdot I_o{}^2 \cdot f}{2}$$

In some cases, this circuit might not provide adequate surge absorption performance since the difference between DC supply voltage E_d and surge voltage makes it an effective solution.

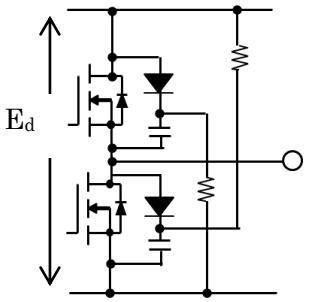


Figure 2.14 Discharge-Suppressing RCD Snubber

L: Stray inductance of the main circuit	I_o: Drain current during device turn-off
C_s: Capacitance of the snubber capacitor	E_d: DC supply voltage
f: Switching frequency	

(2) Lumped snubbers between power buses

a. C snubber

- Although C snubbers are the simplest, they are prone to voltage oscillation due to LC resonance between the stray inductances of the main circuit and the snubber capacitor.

b. RCD snubber

- Care should be exercised as to the selection of a snubber diode since it might cause a high voltage spike as well as voltage oscillation during reverse recovery.

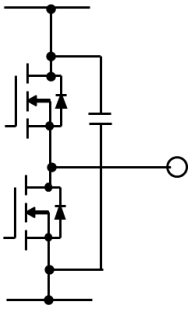


Figure 2.15 C Snubber Circuit

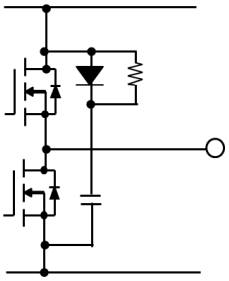


Figure 2.16 RDC Snubber

(3) Creating a snubber design (discharge-suppressing RCD snubber)

Figure 2.17 shows a snubber circuit. Figure 2.18 shows its waveform.

The voltages and circuit constants shown in the waveform can be calculated as follows.

a. V_{DSP1}

V_{DSP1} is voltage produced by the inductance L_s of the snubber and can be calculated as follows:

$$V_{DSP1} = V_{DD} + V_{fr} + L_s \times \frac{di}{dt}$$

It is desirable to minimize the forward voltage V_{fr} of diode D_s. To this end, it is important to reduce L_s that could cause a voltage surge.

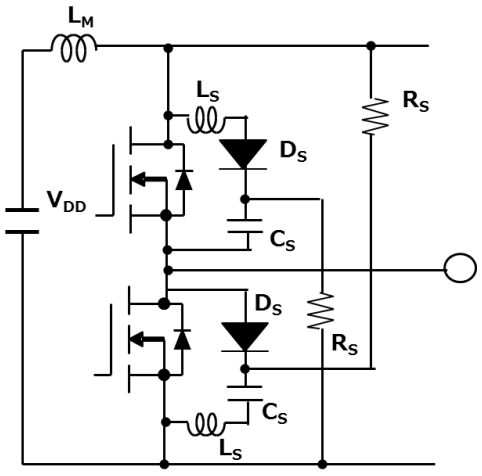


Figure 2.17 Snubber

b. V_{DSP2} and C_s

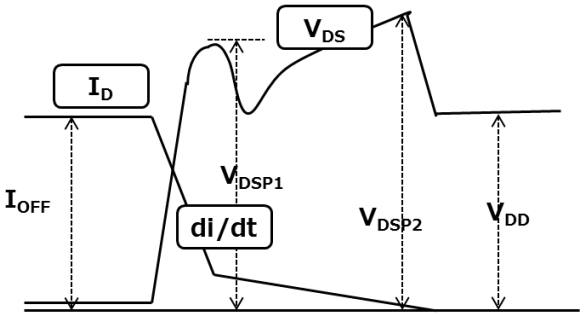
V_{CEP2} is the peak voltage across snubber capacitor C_s that occurs when it is overcharged with the energy from the stray inductance L_M of the main circuit. Since the energy stored in L_M is transferred to C_s, the amounts of their energies are equal. Hence, the following equation holds:

$$\frac{1}{2} \times L_M \times {I_{OFF}}^2 = \frac{1}{2} \times C_s \times (V_{DSP2} - V_{DD})^2$$

From this equation, the value of C_s is calculated as follows:

$$C_s = \frac{L_M \times {I_{OFF}}^2}{(V_{DSP2} - V_{DD})^2}$$

It is necessary to determine the value of V_{DSP2}, considering the withstand voltage of the MOSFET.



L_M : Inductance of main circuit
V_{DD} : Voltage of power supply
L_S : Inductor of snubber circuit
C_S : Capacitor of snubber circuit
R_S : Resistor of snubber circuit
V_{fr} : Forward voltage of Ds
V_{DSP2} : Peak of forward voltage of Cs
V_{DSP1} : Peak of surge voltage by Ls
I_{OFF} : Turn off current
di/dt : Rate of current change

Figure 2.18 Snubber Waveform

c. Selection of the value of snubber resistor Rs

The role of the snubber resistor Rs is to discharge the electric charge stored in the snubber capacitor before a MOSFET begins its next turn-on operation.

Let the discharge time constant be τ, then:

$$\tau = R \cdot C$$

Where, τ is the time taken for the voltage to fall to 37% of the stored voltage.

The time taken for the voltage to fall to 10% (i.e. for the capacitor to discharge 90% of the stored charge) is 2.3τ as shown below.

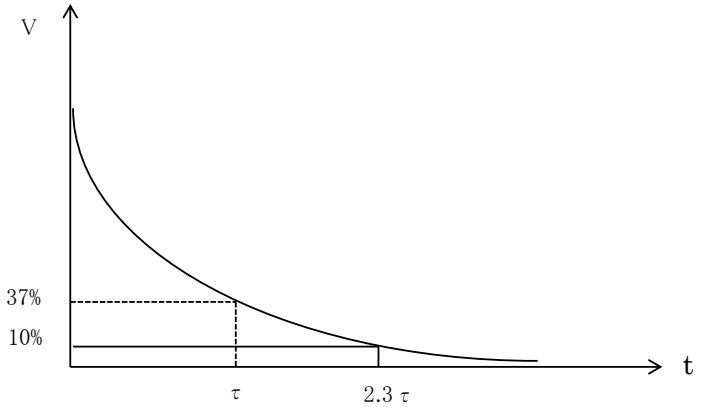


Figure 2.19 Time Constant vs Amount of Discharge

The capacitor must be discharged prior to the next turn-off operation.

Hence, the following equation must be satisfied. From this equation, R_s can be calculated as follows:

$$2.3\tau \leq \frac{1}{f}$$

$$2.3 \times R_s \cdot C_s \leq \frac{1}{f}$$

$$R_s \leq \frac{1}{2.3 \cdot C_s \cdot f}$$

If the value of the snubber resistor is too low, the snubber might exhibit current oscillation. It is necessary to use a resistor with a resistance as high as possible.

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